

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

- 1     1. A method of adjusting carrier mobility for  
2     different semiconductor conductivities on the same  
3     chip comprising steps of  
4         providing a first layer of material providing a  
5     first stress level on a portion of a surface of a  
6     chip,  
7         selectively reducing said first stress level of  
8     a portion of said first layer of material,  
9         providing a second layer of material providing  
10    a second stress level on a portion of a surface of  
11    the chip,  
12         selectively reducing said second stress level  
13    of a portion of said second layer of material.
- 1     2. The method as recited in claim 1 wherein said  
2     first stress level is tensile and said second stress  
3     level is compressive.
- 1     3. The method as recited in claim 1, wherein said  
2     step of providing a first layer is performed by  
3     plasma enhanced chemical vapor deposition.
- 1     4. The method as recited in claim 3, wherein said  
2     first stress level is developed in accordance with  
3     plasma power during said plasma enhanced chemical  
4     vapor deposition.

1       5. The method as recited in claim 1, wherein said  
2       step of providing said second layer is performed by  
3       thermal chemical vapor deposition.

1       6. The method as recited in claim 5, wherein said  
2       step of providing a first layer is performed by  
3       plasma enhanced chemical vapor deposition.

1       7. The method as recited in claim 6, wherein said  
2       first stress level is developed in accordance with  
3       plasma power during said plasma enhanced chemical  
4       vapor deposition.

1       8. The method as recited in claim 1, wherein one of  
2       said first layer of material and said second layer  
3       of material is silicon nitride or silicon  
4       oxynitride.

1       9. The method as recited in claim 1, including the  
2       further step of  
3       forming two transistors in said portion of a  
4       surface of a chip prior to said steps of providing  
5       said first and second layers of material.

1       10. The method as recited in claim 1, wherein said  
2       step of providing a second layer of material results  
3       in a greater thickness than a thickness resulting  
4       from said step of providing a first layer of  
5       material.

1 11. The method as recited in claim 1, wherein said  
2 steps of reducing stress are performed by implanting  
3 ions of germanium, arsenic, xenon, indium,  
4 antimony, silicon, nitrogen oxygen or carbon.

5 12. An integrated circuit comprising  
6 a first circuit element,  
7 a second circuit element,  
8 a first layer of material overlying said first  
9 circuit element and said second circuit element and  
10 having a first stress level in a first region of  
11 said first layer and a second stress level in a  
12 second region of said first layer, and  
13 a second layer of material overlying said first  
14 circuit element and said second circuit element and  
15 having a first stress level in a first region of  
16 said second layer and a second stress level in a  
17 second region of said second layer, wherein said  
18 second stress level in each of said first and second  
19 layers is reduced from the first stress level in  
20 each of said first and second layers.

1 13. The integrated circuit as recited in claim 12,  
2 wherein said first layer and said second layer  
3 comprise an etch stop layer.

1 14. The integrated circuit as recite in claim 12  
2 wherein one of said first layer and said second  
3 layer is one of silicon nitride or silicon  
4 oxynitride.

1     15. The integrated circuit as recited in claim 12,  
2     wherein said first circuit element is a first  
3     transistor and said second circuit element is a  
4     second transistor.

1     16. The integrated circuit as recited in claim 15,  
2     wherein said first and second transistors are field  
3     effect transistors of complementary conductivity  
4     types.

1     17. The integrated circuit as recited in claim 12,  
2     wherein said second region of each of said first and  
3     second layers is implanted with a heavy ion.

1     18. The integrated circuit as recited in claim 17,  
2     wherein said heavy ions are of germanium, arsenic,  
3     xenon, indium, antimony, silicon, nitrogen oxygen or  
4     carbon.

1     19. The integrated circuit as recited in claim 12,  
2     wherein said first layer and said second layer are  
3     of different thickness.

1     20. The integrated circuit as recited in claim 12,  
2     wherein said first stress levels in each of said  
3     first and second layers is in the range of -2.0 to  
4     +2.0 GPa.